REMARKS

Claims 10, 12, and 14 have been amended to address Examiner's concerns. Claims 1-17 remain in the application, although claims 1-9, 11, 13, 15, and 17 have been withdrawn from consideration. A clean copy of the changes is found in Appendix A. Further examination and reconsideration of the application, as amended, is hereby requested.

In Section 2 of the Office Action, the Examiner objected to the drawings because ref. char. 128 in Fig. 5B was not mentioned in the specification. In Section 3 of the Office Action, the Examiner objected to the drawings because they did not contain the ref. char. 126. Applicants have amended the specification to replace the reference character 126 with 128 to make the specification consonant with the drawings. Withdrawal of these two objections is respectfully requested.

In Section 4 of the Office Action, the Examiner objected to the drawings because reference sign 130 in Fig. 5C was not mentioned in the specification. Applicants have amended the specification to include the phrase "to create region 130" to make the specification consonant with the drawings. Withdrawal of this objection is respectfully requested.

In Section 6 of the Office Action, the Examiner rejected claim 10 under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. In particular, the Examiner stated that in "claim 10, line 3 'comprising' should be replaced by –consisting essentially of—unless another step is intended." Also, the Examiner stated that in "claim 10, line 5, it appears that 'consisting essentially of the steps of' should be deleted. Applicants have amended claim 10 as recommended by the Examiner.

In Section 11 of the Office Action, the Examiner indicated that claim 10 would be allowable if rewritten to overcome the rejections under 35 USC 112, second paragraph. Accordingly, Applicants believe claim 10, as amended, is

patentable over the art made of record. Withdrawal of the rejection and allowance of claim 10, as amended, is respectfully requested.

In Section 10 of the Office Action, the Examiner rejected claims 12 and 14 under 35 USC 101 because the disclosed invention is inoperative and therefore lacks utility. In particular, the Examiner asserts that "the step of claim 12, lines 5-8 and claim 14, lines 5-6 is contrary to the step of lines 9-10 and line 7-9, respectively." Applicants respectfully traverse this rejection as the Applicants have built and tested functional devices as claimed and they are indeed operative an provide utility.

As stated in the specification "[i]n conventional IC process, a threshold voltage (V_t) adjusting implant step is used as a control knob to adjust low-voltage CMOS transistor gate threshold voltages." This V_t adjusting implant step requires a V_t protection mask for the high voltage LDMOS transistor (see page 3, lines 14-24). The claimed invention eliminates several process steps used in conventional processes. "The invention simplifies and reduces the cost of conventional processes by redesigning the Well dopant concentrations and foregoing the V_t adjust implant process steps while maintaining substantially the same threshold voltages and breakdown voltages of the conventional processes. Thus, well doping alone is used to control the V_t of the NMOS and PMOS low-voltage transistors" (see page 3, lines 25-31). Applicants believe the Examiner is concerned that threshold *control* of the first steps of each claim is nullified by the additional steps of not including a "voltage threshold *adjust* implant step" as in claim 12 or excluding the step of "implanting a threshold voltage *adjustment*" as in claim 14.

Applicants have amended claims 12 and 14 to more clarify their invention. Claim 12, as amended, now includes the limitation of "wherein *an additional* voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed." Claim 14, as amended, now includes the limitation of excluding the step of "implanting *an additional* threshold voltage adjustment of the first and second low-voltage transistors." Applicants believe that the claims as amended make it clear that and "additional"

threshold voltage adjustment is not performed after the initial voltage threshold setting. These limitations, in combination with the other limitations in their respective claims are not disclosed, taught, or suggested by the art made of record and thus are believed patentable. Withdrawal of the rejection and allowance of claims 12 and 14, as amended, are respectfully requested.

In Section 12 of the Office Action, the Examiner indicated that claim 16 was allowed. Applicants wish to express their appreciation to the Examiner for this allowance.

Applicants believes their claims as amended are patentable over the art of record, and that the amendments made herein are within the scope of a search properly conducted under the provisions of MPEP 904.02. Accordingly, claims 10, 12, 14, and 16 are deemed to be in condition for allowance, and such allowance is respectfully requested.

Respectfully Submitted,
Z. Chen et al.
By: Timothy F Myers 2/19/03
Timothy F. Myers
Patent Attorney
Registration No.
42,919

Hewlett-Packard Company
Legal Department
1000 NE Circle Blvd.
Corvallis, OR 97330
Telephone: (541)715-4197
Fax: (541)715-8581

Appendix A
Clean Copy of Changes

In the Specification:

Please replace the paragraph starting on page 8, line 21 with the following:

A1

Figs. 4A and 4B make up an exemplary flow chart of a modified semiconductor process embodying the invention. Figs 5A through 5M are cross-sectional views of exemplary and some excluded process steps on a substrate 10. The step 50 of Fig. 3A of creating a defined deposition of a first dielectric layer 124 to expose a first region 20 and a second region 22, is illustrated in Fig. 5A. The first dielectric layer 124 can be made of one or more conventional thin film dielectrics. An exemplary first dielectric layer is made up of 200 Angstroms of SRO (stress relief oxide) and 900 Angstroms of silicon nitride. The process step 52 of Fig. 3A can be performed to provide the selective doping of the well regions with essentially the following steps. As shown in Fig 5B and in step 60 of Fig. 4A, a first conductivity dopant of impurities 128 is implanted into the first and second 20/22 regions. An exemplary N-Well implant is 2.8 to 3.0 x 10^{12} impurities/cm^2 of phosphorous at 160 keV of energy. Then in step 62 and Fig. 5C, a first protective coating 132 is applied over the first and second 20/22 regions. An exemplary first protective coating is field oxide (FOX). Then in step 64 and Fig. 5C, the first conductivity dopant 128 is driven into the substrate to form regions 132 by baking the substrate 10, such as at 1200°C for 4 hours. Then in step 66, the first dielectric layer 124 is removed. Then in step 68 and Fig. 5D, a defined deposition of a second dielectric layer 136 is created in the same location as the defined deposition of the first dielectric layer 124, such as channel oxide. Then in step 70 and Fig. 5D, a second conductivity dopant 138 is implanted in the substrate 10 as second conductivity implant 134 and disposed under the defined deposition of the second dielectric layer 136. An exemplary second conductivity dopant 138 is boron at a concentration of 9.8 x 10^{12} impurities/cm^2 at an energy of 33 keV. Then in step 72 and Fig. 5E, the second conductivity implant 134 is driven into the substrate10 to form a driven second conductivity implant 140, preferably by

baking the substrate 10 at 1200°C at 4 hours. Then in step 74 and Fig. 5E, the first protective coating 132 and the second dielectric layer 136 are removed, for example, by using an oxide strip. Then in step 76 and Fig. 5F, a patterned third dielectric layer 146 is created over the surface of the substrate to expose the drain and source of the first 28 and second 26 conductivity low-voltage transistors and the first conductivity high-voltage transistor 30. The third dielectric layer 146 can be made of one or more dielectric layers. An exemplary third dielectric layer is made up of 200 Angstroms of SRO and 900 Angstroms of silicon nitride. Then in step 78, a defined deposition of a fourth dielectric layer 148 is created and disposed on the drain and source of the first conductivity low-voltage transistor 28. Then in step 80 and Fig. 5G, a second protective coating 150, for example photoresist, is applied over the first 142 and second 144 wells. Then in step 82 and Fig. 5H, a second conductivity field dopant 152 is implanted into the substrate and disposed under the drain and source of the first conductivity low-voltage transistor 28. An exemplary concentration of the second conductivity field dopant 152 is boron at a concentration of 8.5×10^{12} impurities/cm^2 at and energy of 120 keV. Then in step 84, the second protective coating 150 is removed. Then in step 86 and Fig. 5I, a fifth dielectric layer 154, for example FOX, is created in areas of the substrate where the third dielectric layer 146 is not located. Then in step 88, the patterned third dielectric layer 146 is removed, for example with an oxide strip.

In the Claims:

10. (Amended) A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, consisting essentially of the steps of:

creating a defined deposition of a first dielectric layer to expose a first region and a second region;

implanting a first conductivity dopant into the first and second regions;

applying a first protective coating over the first and second regions;

driving in the first conductivity dopant into the substrate;

removing the first dielectric layer;

creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer;

implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer;

driving in the second conductivity dopant into the substrate;

removing the first protective coating and the second dielectric layer;

creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor;

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor;

applying a second protective coating over the first and second regions;

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor;

removing the second protective coating;

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located;

removing the patterned third dielectric layer; and

then further comprising the steps of:

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

12. (Amended) A method of creating an integrated circuit having a second conductivity low-voltage transistor in a first region, a first conductivity high-voltage transistor in a second region, and a first conductivity low-voltage transistor in a third region, comprising the steps of:

doping the first and second regions with a first dopant concentration to control the threshold voltage of the second conductivity low-voltage transistor; and

doping the third region with a second dopant concentration to control the threshold voltage of the first conductivity low-voltage transistor;

wherein an additional voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed.

14. (Amended) A method of processing an integrated circuit having a second conductivity low-voltage transistor in a first region, a first conductivity high-voltage transistor in a third region, and a first conductivity low-voltage transistor in a second region, comprising the steps of:

doping the first and second regions with a first dopant concentration; and

doping the third region with a second dopant concentration; and

excluding the step of:

implanting an additional threshold voltage adjustment of the first and second low-voltage transistors; and

wherein the first and second regions have the substantially the same dopant concentration after processing of the integrated circuit.